Remarks

Applicant respectfully requests reconsideration of this application as new. Claims 1-4, 16-18, 38 and 39 have been amended. No claims have been cancelled. Therefore claims 1-28 and 38-49 are presented for examination.

In a Final Office Action mailed April 18, 2002, claims 1-28 and 38-49 stand rejected under 35 U.S.C. 102(b) as being anticipated by Direct Rambus Technology Disclosure ("Rambus Disclosure"). Applicants submit that the present claims are patentable over the Rambus Disclosure.

The Rambus Disclosure discloses a memory controller coupled to Rambus DRAMs via a Rambus Channel. The memory controller contains intelligence and a Rambus Interface that converts from low-swing voltage levels used by the Rambus Channel to ordinary CMOS logic levels. See Rambus Disclosure at page 7, column 2. In addition, the Rambus memory controller supports all control functions including protocol, refresh, memory and interleaving support (page 14, col. 2).

Claim 1 recites a refresh timing circuit to compensate for operating conditions in a computer system by evaluating time between memory refresh events when the computer system is operating in a normal mode. Applicants submit that nowhere in the Rambus Disclosure is such a refresh timing circuit disclosed. Consequently, claim 1 is patentable over the Rambus Disclosure.

Claims 2-15 depend from claim 1 and include additional limitations. Therefore, claims 2-15 are also patentable over the Rambus Disclosure.

Claim 15 recites a refresh timing circuit to compensate for operating conditions in a computer system by evaluating time between memory refresh events when the

computer system is operating in a normal mode. Thus, for the reasons stated above with respect to claim 1, claim 16 is also patentable over the Rambus Disclosure. Because claims 17-28 depend from claim 16 and include additional limitations, claims 17-28 are also patentable over the Rambus Disclosure.

Claim 38 recites an internal clock generator having a host clock refresh counter to reference a host clock signal to generate memory refresh events whenever a computer system is operating in a normal mode, and a clock generator to generate clock signals to generate clock signals to trigger the memory refresh events whenever the computer system is operating in the low power mode. Applicants submit that the Rambus Disclosure does not disclose a host clock refresh counter to reference a host clock signal to generate memory refresh events whenever a computer system is operating in a normal mode, and a clock generator to generate clock signals to generate clock signals to trigger the memory refresh events whenever the computer system is operating in the low power mode. Thus, claim 38 is also patentable over the Rambus Disclosure. Since claims 39-49 depend from claim 28 and include additional limitations, claims 39-49 are also patentable in view of the Rambus Disclosure.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date:_____

_____

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980